Synthetic presentation of the major clusters in nanoelectronics

Charles Collet, GAEL,
October 07

Introduction

- Nanoelectronics can be considered as an exception in nanosciences :
- it's indeed a nanotechnology (producing devices at the nanoscale), but its top down approach, as a continuation of the microelectronics roadmap, doesn't constitue -yet- a breakthrough as it doesn't bring changes in physical properties.
- It's a nanotechnology but not a nanoscience, yet.

UMR GAEL

- Comparing & positioning nanoelectronics clusters is a hard task due to heterogeneity of their activities.

- Indeed the current split of their business models (continuation of miniaturization, diversification on new functionalities) makes it for example irrelevant to compare nb of employees (front vs back end) or investment.

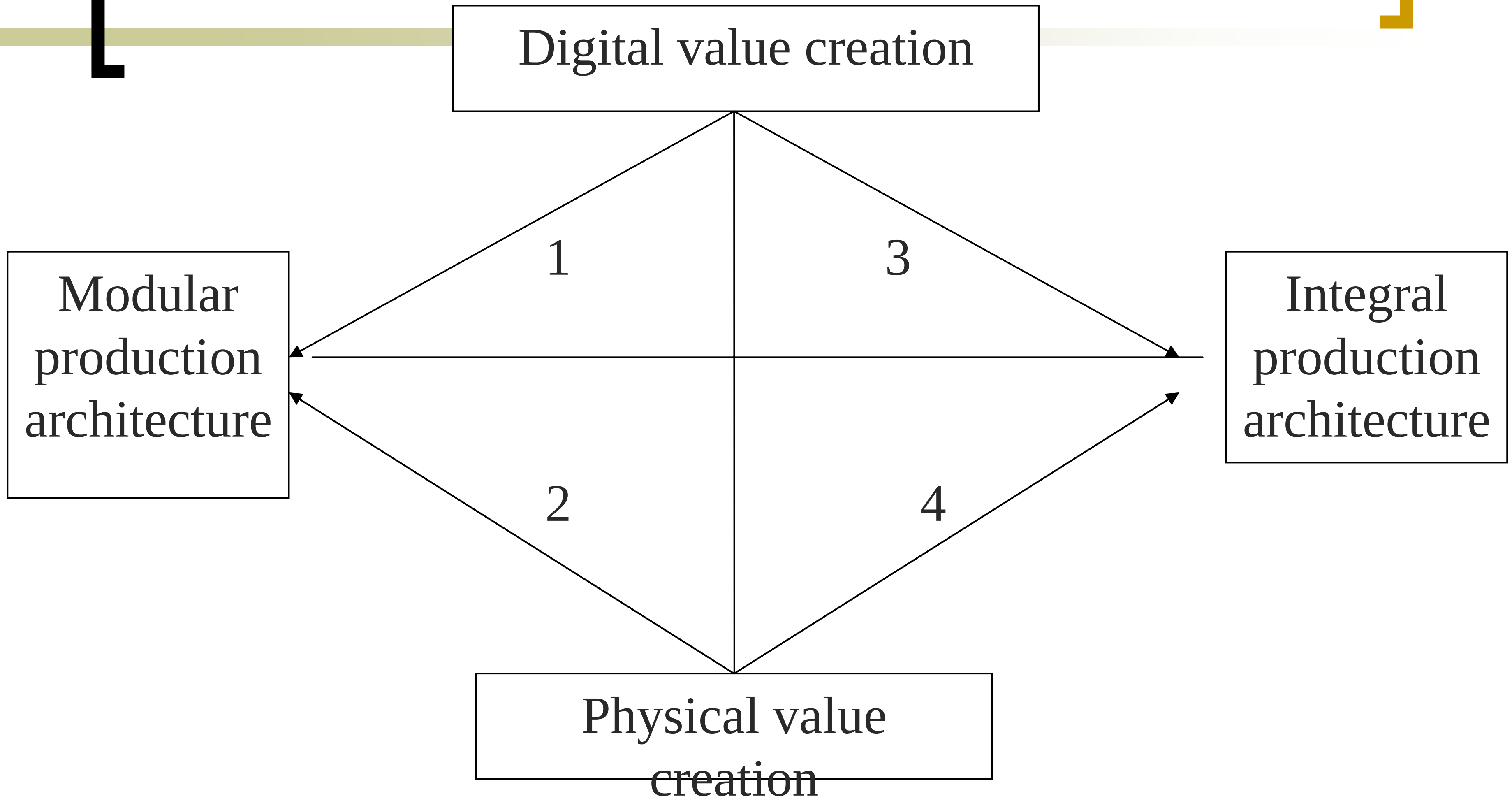
- The only criterion that is however common to growing clusters seems to be the excellence of their applied research
- We can thus present the repartition of the industry, major clusters in their position on the value chain.

UMR GAEL

global world: a need for innovation versus a push for production relocation.

- 2 axis in Business Model Change:
- **Digital versus Physical** Value Added (design vs production)
- **Modular versus Integral architecture:** miniaturized & standardized chips (More Moore) vs miniaturized & specific chips (More than Moore)

UMR GAEL


Digital value creation
Modular production architecture
Integral production architecture
Physical value creation
1
2
3
4

- 1) digital & modular: value added is on design, & the architecture design is modular
- *→IP providers designing the process'cores or ASICs(like ARM, MIPS)*
- IP providers conceive generic chips' cores around which other firms (fabless or IDMs) will design some extended architectures for specific applications.
- coordination costs are low (IP providers just have to send the digital architecture to other fabless or IDMs), & the IP can be understood by any manufacturer

- 2) physical & modular : mass production of generic chips (high volume/low unit value)
- *→ the pure play foundries Business Model for chips & memories (TSMC, UMC, Qimonda, etc)*
- *VA is indeed physical (chip production that involves a high capital intensity), & the production model is modular, as these firms produce chips that will be sold to different customers & integrate a large range of products.*
- R&D costs are heavily supported by manufacturers as their competitive advantage relies on the ability to keep on with miniaturization (More Moore)

UMR GAEL

- 3) digital & integral : Value on design, specific architectures & new functionalities.
- → the Fabless Business Model (Broadcom, Qualcomm, IBM, Freescale, etc)
- value added is even more digital & knowledge-intensive, as these design companies conceive specific chips for specific clients, which will be produced by foundries.
- chips are specific & can’t be applied to different products, thus taking place in an integral production strategy.

UMR GAEL

4) physical & specific : complex systems produced by IDMs & integrative clusters:

→ the Integrated Business Model (TI, Samsung, STM, Grenoble, Dresde, Albany clusters,)etc

- VA is on design & also on production of these specific chips like NEMS (Nano Electronics Mechanical Systems), as the complexity of the chip makes production as knowledge intensive as the design.

- labs-on-chip, Embedded System on Chip, Secured Solutions, NEMS, etc.

UMR GAEL

Valeur plutôt « digitale »

Production de puces standards / modulaires (VA faible, production de masse)

1-IP providers qui conçoivent un cœur de process: ARM, MIPS, etc

3- designers « fabless » : Qualcomm, Broadcom, etc, & orientation prise par NXP, FSL pour les générations < 45nm

2- producteurs de masse « More Moore » : Dresde (Qimonda,), &Taiwan (fonderies), fabricants de mémoires : Epida, Powerchip, etc.

4- entreprises intégratrices : ST, TI, Atmel, etc & clusters produisant des solutions intégrées, labos sur puce, etc: Grenoble, Eindhoven, Albany.

Production de puces spécialisées ou intégrées (VA forte, prod de lignes limitées)

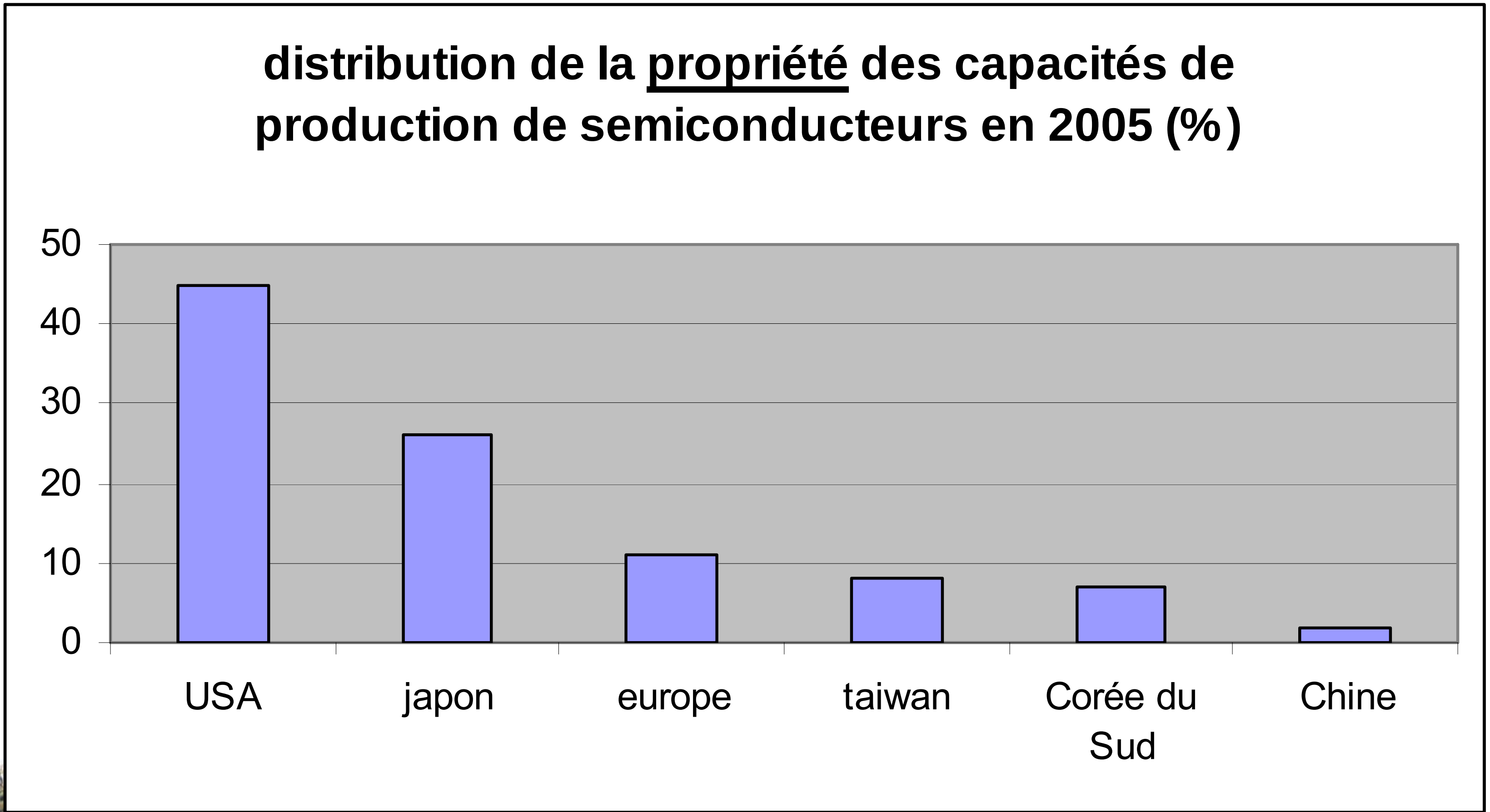
Valeur plutôt « physique »

UMR GAEL

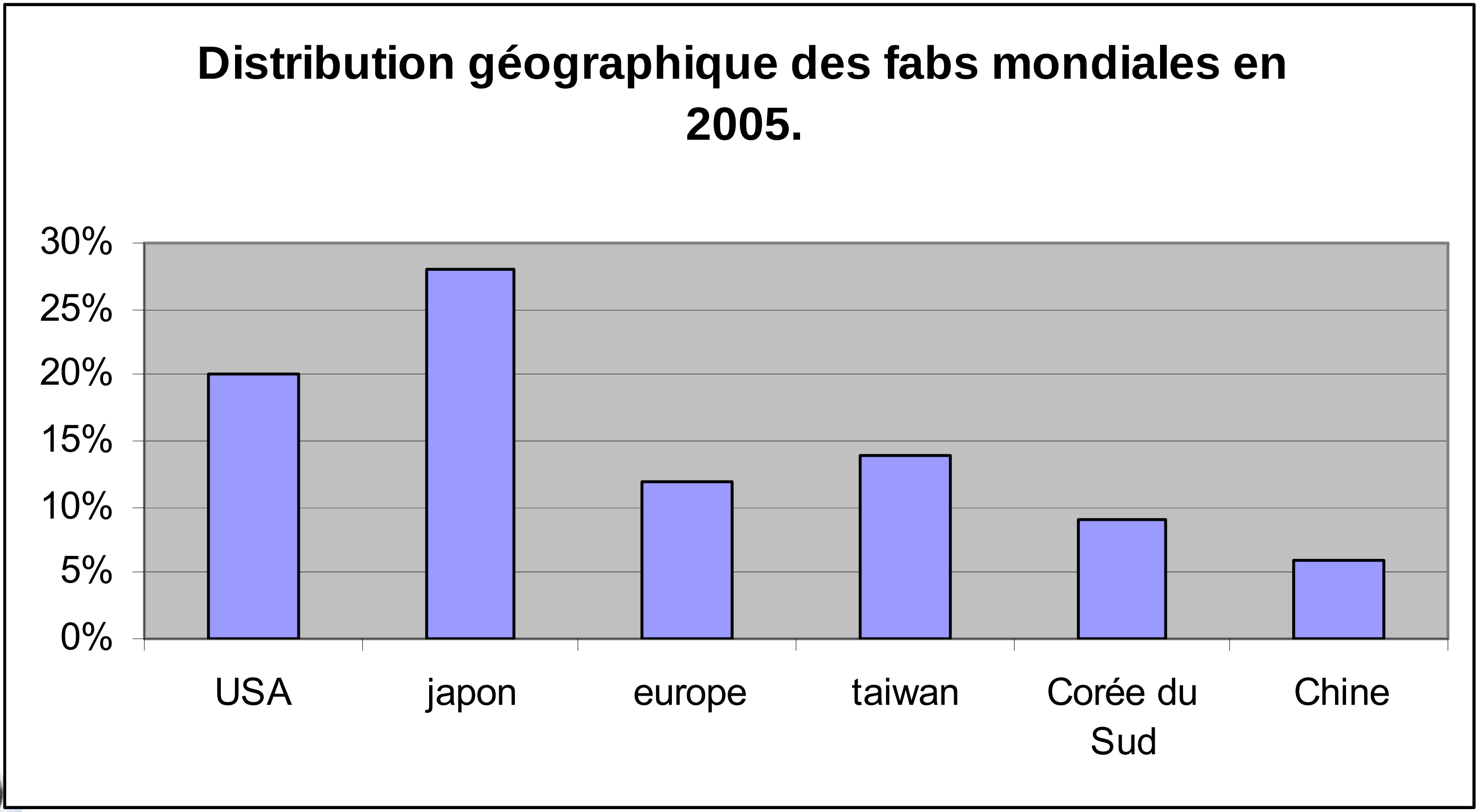
Structure of the clusters around a double anchor

	Grenoble	Dresde	Louvain/Eindhoven	Albany	Taiwan
Anchor tenant firm	STM	Infineon, AMD	NXP	IBM, Samsung, AMD, Micron, Infineon, Chartered.	TSMC, UMC
Research Lab	CEA Léti	CNT	IMEC	CNSE	ITRI
Nombre d'employés	20 000	20 000	25 000	50 000	76 000
Business Model & Positionning	Recherche locale forte & intégration multidisciplinaire (Minatec)	Recherche locale & production de masse (processeurs, mémoires)	Recherche internationale & design diversifié	Recherche internationale & intégration multidisciplinaire	Production de masse
Type of Value Added	Digitale & architectures spécialisées	Physique, architectures modulaires & spécialisées	Digitale & architectures spécialisées	Digitale, architectures modulaires & spécialisées	Physique, architectures modulaires

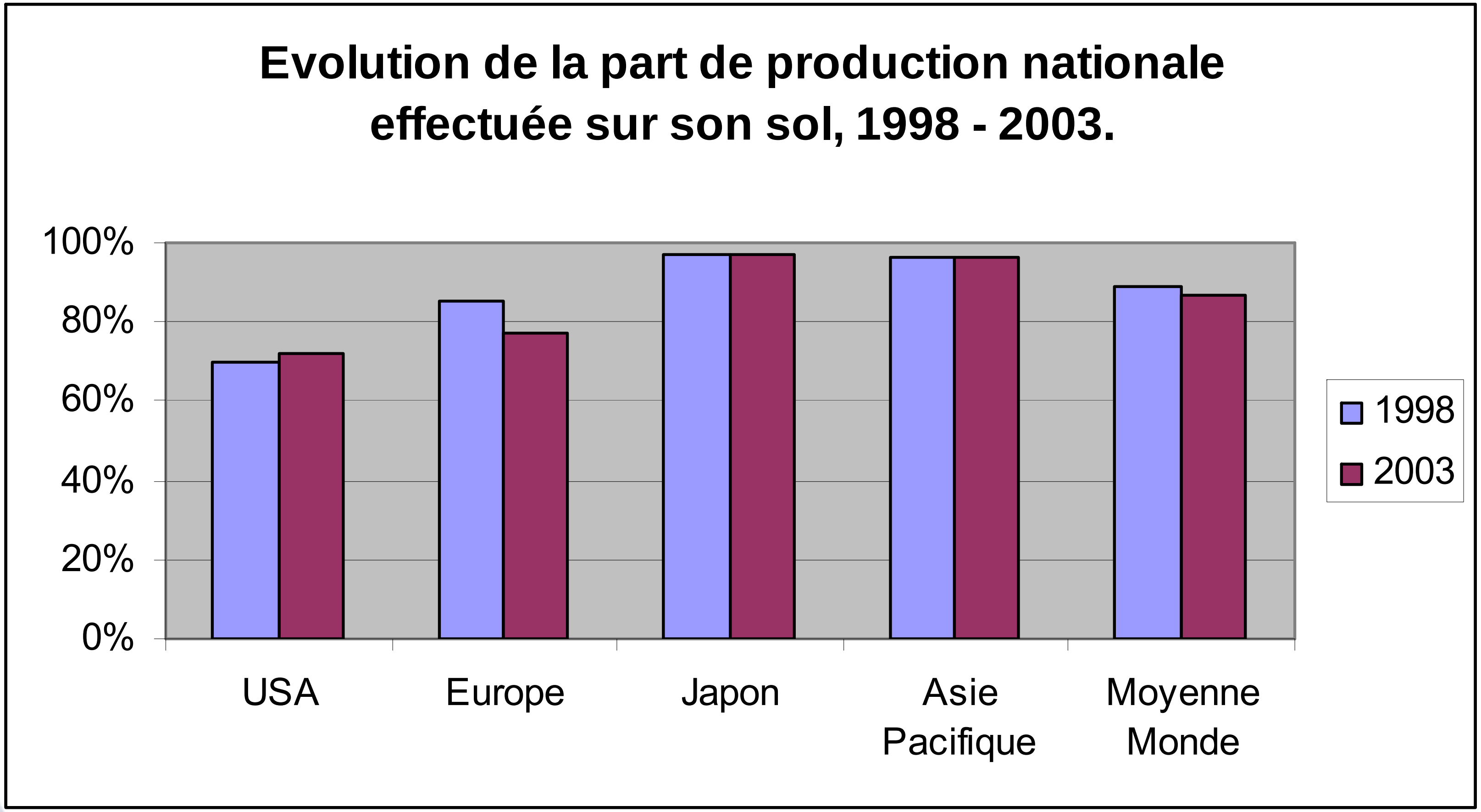
Repartition of production capacities' ownership, nanoelectronics.



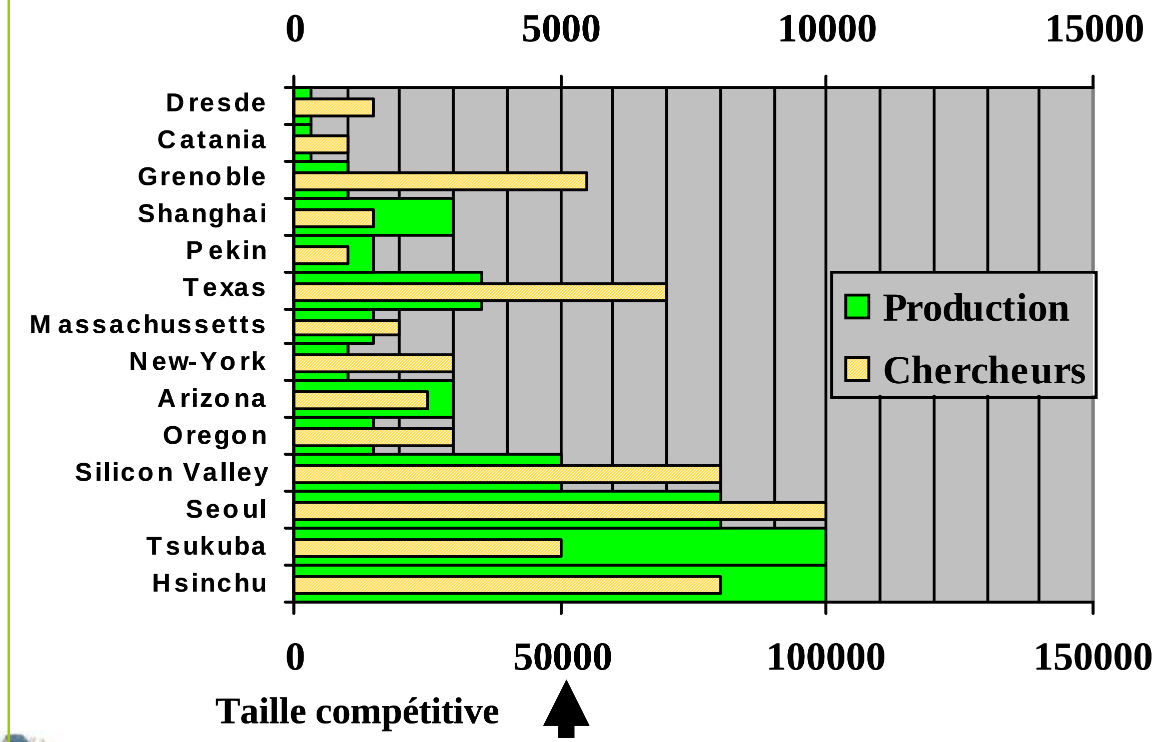
Repartition of production capabilities locations, nanoelectronics.



Evolution of the national production produced inshore



Number of dedicated researchers & operational workers in nanoelectronics clusters, ex of Grenoble.

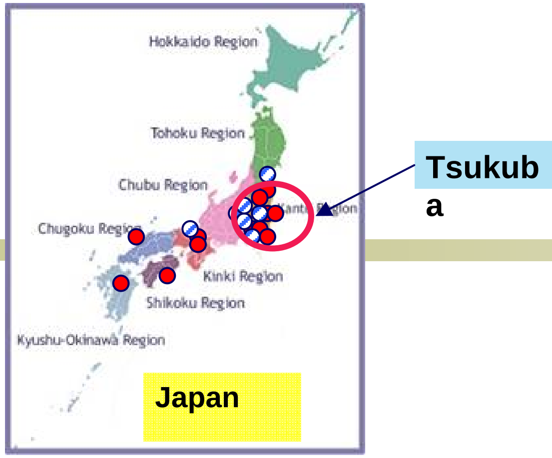


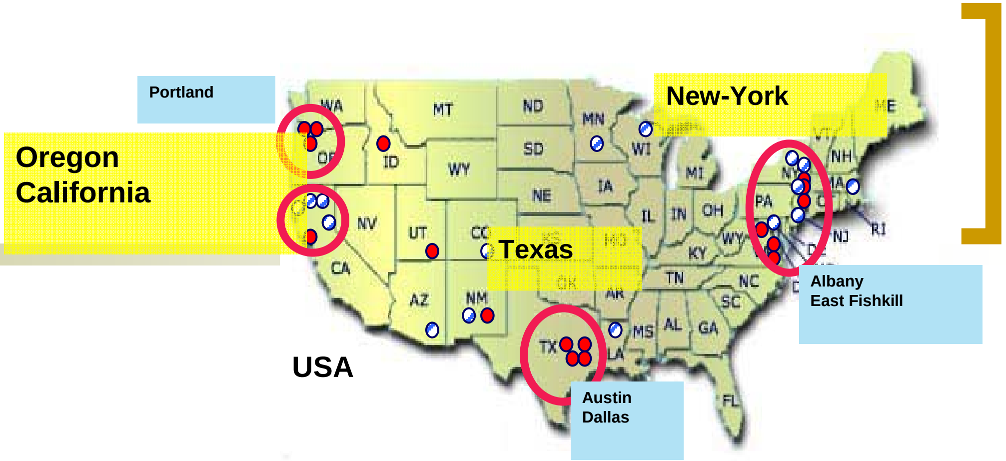
Le pôle Grenoblois a une taille compétitive en matière de recherche

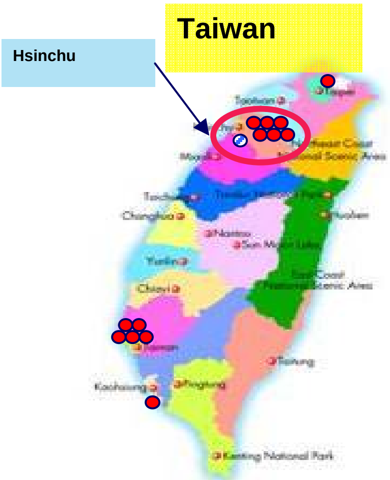
➔ il lui faut encore acquérir la dimension de production industrielle adéquate

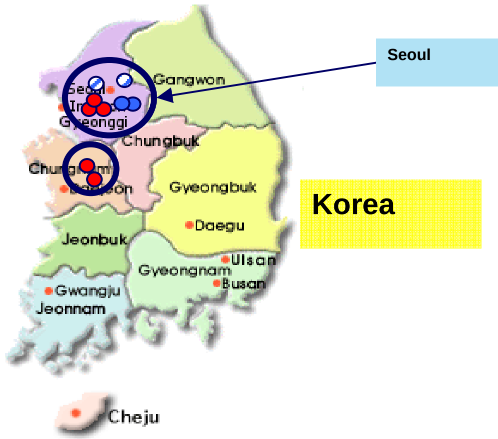
UMR GAEL

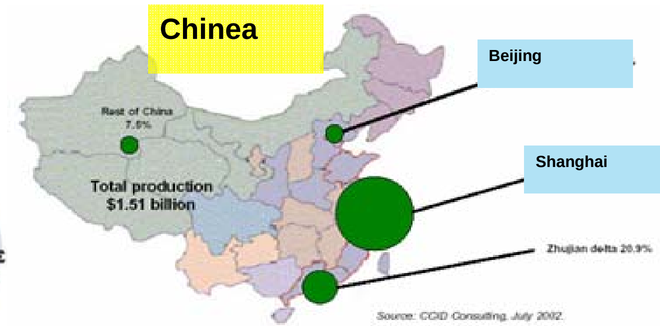
Competitiors of European clusters







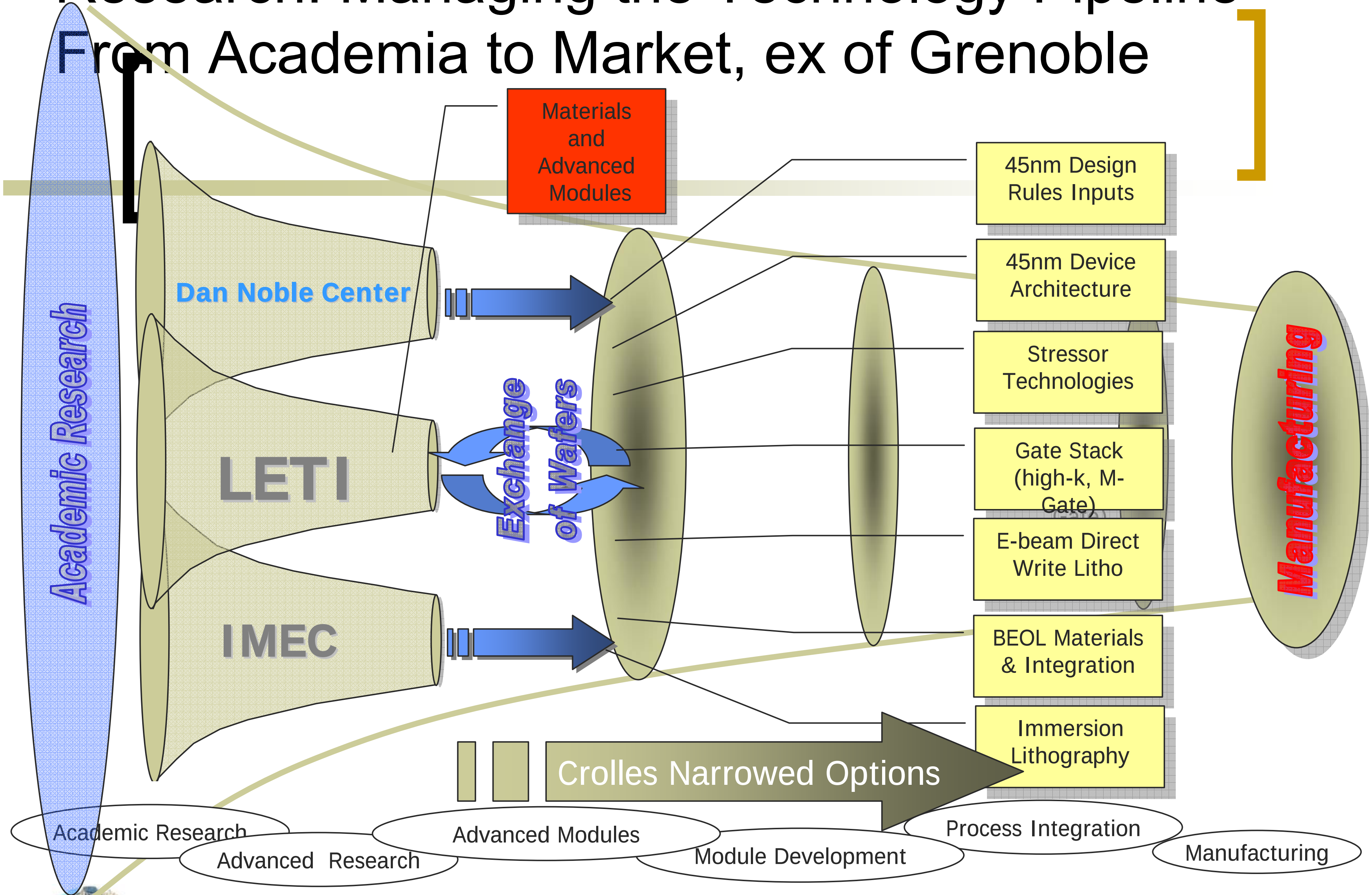




Fab 300 mm Fabs

Labo Public

Research: Managing the Technology Pipeline
From Academia to Market, ex of Grenoble



UMR GAEL

Conclusion: Successful clusters in high cost regions rely on differentiating themselves from their competition

- Europe may be loosing the cost war for low value-adding industries, but not the same for high tech & capital-intensive sectors such as nanoelectronics, as in this high tech industry the cost of equipment (clean rooms, lithography tools) & workforce (engineers) became similar globally.
- however the differences between territories mainly rely on state subsidies & tax regimes. Taiwan or China wouldn't have been able to build their competitive foundries without a public support being higher than the one granted in Europe & US together for the same time period (about 4 billion $ between 2002-2007). That shows that with a same amount of subsidies & a same tax rate European nanoelectronics clusters like Dresden or Grenoble would surely be as competitive as Taiwan, all things remaining equal.
- This statement goes against the common acceptation saying that if their ability to make a good becomes ubiquitous, the competitive advantage of European clusters should shift from the production line to management strategies, innovation, R&D, or marketing (Andersen, 2005).
- But what we do agree with, is that without the same national or environmental conditions the challenge for western clusters is to reinvent themselves in ways that keep a level of local employment, as it will be hard for them to compete on production with places that have the combination of now skilled labor forces, strong political help &

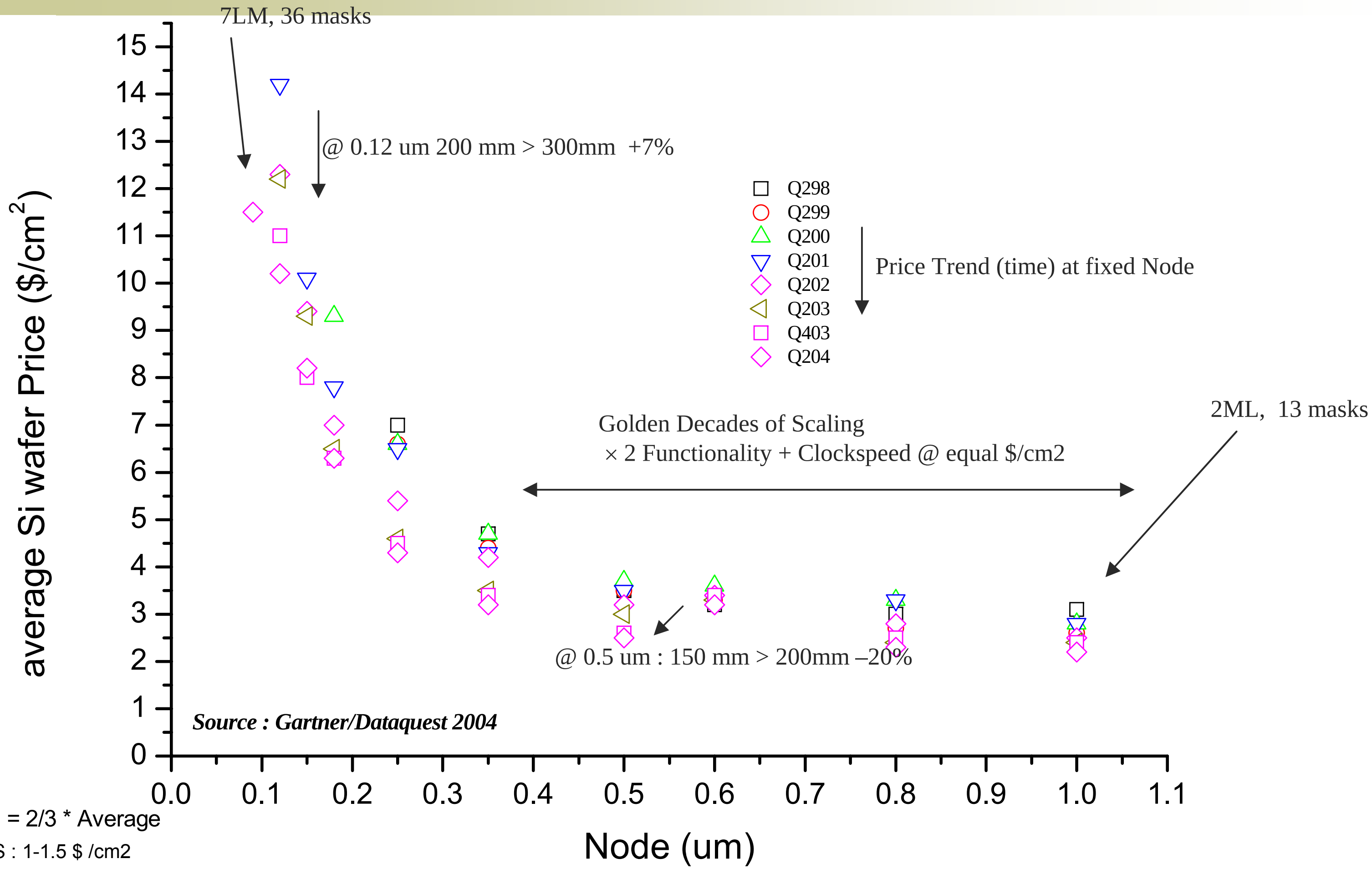
- Most strategies have looked to the universities as the source of new and distinguishing innovations, & most cluster analyses include rates of patents and publications as evidence of innovation.
- But for these indicators Taiwanese cluster again do as good as European ones. The difference between Asian & western clusters is the fact that they have been built on a longer tradition & already developed secondary competencies, like biotechnology in Grenoble, Dresden or Albany-Boston, which now can really become a source of advantage in the convergence enabled at the nanoscale.
- “Creative Centers,” Richard Florida writes, “tend to be the economic winners of our age.” These creative centers have the attributes—physical, diversity, and experiences—to attract what he defines as the creative class. & it’s up to this creative class now to design complex & integrated systems so as to swift the value from low cost to high performance, & diversify on new functionalities so as to create new value.

UMR GAEL

Actor	Goal	Advantage
Foundries	Making chips smaller & cheaper	low cost thanks to mass production, investment in miniaturization
Fabless / Design firms	Designing chips better	Miniaturized architecture, low consumption &/or high performance
Integrative firms & clusters	Designing better chips	Bridging disciplines & competencies to develop new & high value adding solutions

Table: competitive advantage of the micro/nanoelectronics actors, Charles Cellet, 2007.

Those Golden Days of Scaling: Pricetrend Baseline CMOS



Min = 2/3 * Average

LTPS : 1-1.5 $ /cm2

Source: [2005] Carel van der Poel, Philips Research

UMR GAEL